ANNA UNIVERSITY, CHENNAI

AFFILIATED INSTITUTIONS

R- 2009

CURRICULUM I SEMESTER (FULL TIME)

M.E. APPLIED ELECTRONICS

SEMESTER I

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1	**MA9217**	Applied Mathematics for Electronics Engineers	3	1	0	4
2	AP9211	Advanced Digital Signal Processing	3	0	0	3
3	AP9212	Advanced Digital System Design	3	0	0	3
4	VL9212	VLSI Design Techniques	3	0	0	3
5	AP9213	Advanced Microprocessors and Micro Controllers	3	0	0	3
	E1	Elective I	3	0	0	3
PRACTICAL						
6	AP9217	Electronics Design Lab I	0	0	4	2
		TOTAL	**18**	**1**	**4**	**21**

LIST OF ELECTIVES

M.E. APPLIED ELECTRONICS

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
1	**AP9251**	**Digital Image Processing**	**3**	**0**	**0**	**3**
2	AP9252	Neural Networks and Its Applications	3	0	0	3
3	AP9253	ROBOTICS	3	0	0	3
4	VL9211	DSP Integrated Circuits	3	0	0	3
5	VL9261	ASIC Design	3	0	0	3
6	AP9260	Design and Analysis of Algorithms	3	0	0	3
7	NE9251	Reliability Engineering	3	0	0	3
8	AP9256	Electromagnetic Interference and Compatibility in System Design	3	0	0	3
9	CP9212	High Performance Computer Networks	3	0	0	3
10	AP9258	RF system Design	3	0	0	3
11	VL9252	Low Power VLSI Design	3	0	0	3
12	VL9253	VLSI Signal Processing	3	0	0	3
13	VL9254	Analog VLSI Design	3	0	0	3
14	VL9221	CAD for VLSI Circuits	3	0	0	3
15	AP9259	Hardware Software Co-design	3	0	0	3
16		Special Elective	3	0	0	3

MA9217 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS **L T P C 3 1 0 4**

UNIT I FUZZY LOGIC **12**

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II MATRIX THEORY **12**

Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition - Toeplitz matrices and some applications.

UNIT III ONE DIMENSIONAL RANDOM VARIABLES **12**

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT IV DYNAMIC PROGRAMMING **12**

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V QUEUEING MODELS **12**

Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula - Machine Interference Model – Steady State analysis – Self Service queue.

L = 45: T=15; TOTAL: 60 PERIODS

REFERENCES:

1. George J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt. Ltd., 1997.
2. Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing, Pearson Education, 2000.
3. Richard Johnson, Miller & Freund's Probability and Statistics for Engineers, 7th Edition, Prentice – Hall of India, Private Ltd., New Delhi (2007).
4. Taha, H.A., Operations Research, An introduction, 7th edition, Pearson education editions, Asia, New Delhi, 2002.
5. Donald Gross and Carl M. Harris, Fundamentals of Queuing theory, 2nd edition, John Wiley and Sons, New York (1985).

AP9211 ADVANCED DIGITAL SIGNAL PROCESSING **L T P C 3 0 0 3**

UNIT I DISCRETE RANDOM SIGNAL PROCESSING **9**

Discrete Random Processes- Ensemble Averages, Stationary processes, Bias and Estimation, Autocovariance, Autocorrelation, Parseval's theorem, Wiener-Khintchine relation, White noise, Power Spectral Density, Spectral factorization, Filtering Random Processes, Special types of Random Processes – ARMA, AR, MA – Yule-Walker equations.

UNIT II SPECTRAL ESTIMATION 9

Estimation of spectra from finite duration signals, Nonparametric methods - Periodogram, Modified periodogram, Bartlett, Welch and Blackman-Tukey methods, Parametric methods – ARMA, AR and MA model based spectral estimation, Solution using Levinson-Durbin algorithm

UNIT III LINEAR ESTIMATION AND PREDICTION 9

Linear prediction – Forward and Backward prediction, Solution of Prony's normal equations, Least mean-squared error criterion, Wiener filter for filtering and prediction, FIR and IIR Wiener filters, Discrete Kalman filter

UNIT IV ADAPTIVE FILTERS 9

FIR adaptive filters – adaptive filter based on steepest descent method- Widrow-Hopf LMS algorithm, Normalized LMS algorithm, Adaptive channel equalization, Adaptive echo cancellation, Adaptive noise cancellation, RLS adaptive algorithm.

UNIT V MULTIRATE DIGITAL SIGNAL PROCESSING 9

Mathematical description of change of sampling rate – Interpolation and Decimation, Decimation by an integer factor, Interpolation by an integer factor, Sampling rate conversion by a rational factor, Polyphase filter structures, Multistage implementation of multirate system, Application to subband coding – Wavelet transform

TOTAL: 45 PERIODS

REFERENCES:

1. Monson H. Hayes, 'Statistical Digital Signal Processing and Modeling", John Wiley and Sons, Inc, Singapore, 2002
2. John J. Proakis, Dimitris G. Manolakis, : Digital Signal Processing', Pearson Education, 2002
3. Rafael C. Gonzalez, Richard E. Woods, " Digital Image Processing", Pearson Education Inc.,Second Edition, 2004 (For Wavelet Transform Topic)

AP9212 ADVANCED DIGITAL SYSTEM DESIGN L T P C
3 0 0 3

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits-design of iterative circuits-ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method-path sensitization method – Boolean difference method-D algorithm -Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

UNIT V SYSTEM DESIGN USING VHDL 9

VHDL operators – Arrays – concurrent and sequential statements – packages- Data flow – Behavioral – structural modeling – compilation and simulation of VHDL code –Test bench - Realization of combinational and sequential circuits using HDL – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor

TOTAL : 45 PERIODS

REFERENCES:

1. Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004
2. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001
3. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002
4. Parag K.Lala “Digital system Design using PLD” B S Publications,2003
5. Charles H Roth Jr.”Digital System Design using VHDL” Thomson learning, 2004
6. Douglas L.Perry “VHDL programming by Example” Tata McGraw.Hill - 2006

VL9212 VLSI DESIGN TECHNIQUES L T P C
3 0 0 3

UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY 9

NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.

UNIT II INVERTERS AND LOGIC GATES 9

NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III CIRCUIT CHARACTERIZATION AND PERFORMANCE ESTIMATION 9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN 9

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modelling ,cross talk, floor planning, power distribution. Clock distribution. **Basics of CMOS testing**.

UNIT V VERILOG HARDWARE DESCRIPTION LANGUAGE 9

Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.

TOTAL : 45 PERIODS

REFERENCES:

1. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
2. John P.Uyemura "Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc., 2002.
3. Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Edition, 2004.
4. Eugene D.Fabricius, "Introduction to VLSI Design", McGraw Hill International Editions, 1990.
5. J.Bhasker, B.S.Publications, "A Verilog HDL Primer", 2nd Edition, 2001.
6. Pucknell, "Basic VLSI Design", Prentice Hall of India Publication, 1995.
7. Wayne Wolf "Modern VLSI Design System on chip. Pearson Education.2002.

AP9213 ADVANCED MICROPROCESSORS AND MICROCONTROLLERS L T P C
3 0 0 3

UNIT I MICROPROCESSOR ARCHITECTURE 9

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC**.**

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 9

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM 9

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV MOTOROLA 68HC11 MICROCONTROLLERS 9

Instruction set addressing modes – operating modes- Interrupsystem- RTC-Serial Communication Interface – A/D Converter PWM and UART.

UNIT V PIC MICROCONTROLLER 9

CPU Architecture – Instruction set – interrupts- Timers- I^2C Interfacing –UART- A/D Converter –PWM and introduction to C-Compilers.

TOTAL : 45 PERIODS

REFERENCES :

1. Daniel Tabak , ‘’ Advanced Microprocessors” McGraw Hill.Inc., 1995
2. James L. Antonakos , “ The Pentium Microprocessor ‘’ Pearson Education , 1997.
3. Steve Furber , ‘’ ARM System –On –Chip architecture “Addision Wesley , 2000.
4. Gene .H.Miller .” Micro Computer Engineering ,” Pearson Education , 2003.
5. John .B.Peatman , “ Design with PIC Microcontroller , Prentice hall, 1997.
6. James L.Antonakos ,” An Introduction to the Intel family of Microprocessors ‘’ Pearson Education 1999.
7. Barry.B.Breg,” The Intel Microprocessors Architecture , Programming and Interfacing “ , PHI,2002.
8. Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprint 2001.

AP9217 ELECTRONICS DESIGN LABORATORY I L T P C
0 0 4 2

1. System design using PIC Microcontroller.
2. Implementation of Adaptive Filters, periodogram and multistage multirate system in DSP Processor
3. Simulation of QMF using Simulation Packages
4. Modeling of Sequential Digital system using VHDL.
5. Modeling of Sequential Digital system using Verilog.
6. Design and Implementation of ALU using FPGA.
7. Simulation of NMOS and CMOS circuits using SPICE.
8. System design using 16- bit Microprocessor.

TOTAL : 60 PERIODS

AP9251 DIGITAL IMAGE PROCESSING L T P C
3 0 0 3

UNIT I DIGITAL IMAGE FUNDAMENTALS 9

Elements of digital image processing systems, Vidicon and Digital Camera working principles, Elements of visual perception, brightness, contrast, hue, saturation, Mach Band effect, Image sampling, Quantization, Dither, Two dimensional mathematical preliminaries.

UNIT II IMAGE TRANSFORMS 9

1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

UNIT III IMAGE ENHANCEMENT AND RESTORATION 9

Histogram modification, Noise distributions, Spatial averaging, Directional Smoothing, Median, Geometric mean, Harmonic mean, Contraharmonic and Yp mean filters . Design of 2D FIR filters. Image restoration - degradation model, Unconstrained and Constrained restoration, Inverse filtering-removal of blur caused by uniform linear motion, Wiener filtering, Geometric transformations-spatial transformations, Gray Level interpolation. .

UNIT IV IMAGE SEGMENTATION AND RECOGNITION 9

Image segmentation - Edge detection, Edge linking and boundary detection, Region growing, Region splitting and Merging, Image Recognition - Patterns and pattern classes, Matching by minimum distance classifier, Matching by correlation., Neural networks-Backpropagation network and training, Neural network to recognize shapes.

UNIT V IMAGE COMPRESSION 9

Need for data compression, Huffman, Run Length Encoding, Shift codes, Arithmetic coding, Vector Quantization, Block Truncation Coding, Transform coding, JPEG standard, JPEG 2000, EZW, SPIHT, MPEG.

TOTAL: 45 PERIODS

REFERENCES:

1. Rafael C. Gonzalez, Richard E. Woods, " Digital Image Processing", Pearson Education, Inc., Second Edition, 2004
2. Anil K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall of India, 2002.
3. Rafael C. Gonzalez, Richard E. Woods, Steven Eddins," Digital Image Processing using MATLAB", Pearson Education, Inc., 2004.
4. D.E. Dudgeon and R.M. Mersereau, "Multidimensional Digital Signal Processing", Prentice Hall Professional Technical Reference, 1990.
5. William K. Pratt, " Digital Image Processing", John Wiley, New York, 2002.
6. Milan Sonka et al, "Image Processing, Analysis and Machine Vision", Brookes/Cole, Vikas Publishing House, 2nd edition, 1999;
7. Sid Ahmed, M.A., " Image Processing Theory, Algorithms and Architectures", McGrawHill, 1995.

AP9252 NEURAL NETWORKS AND ITS APPLICATIONS L T P C
3 0 0 3

UNIT I BASIC LEARNING ALGORITHMS 9

Biological Neuron – Artificial Neural Model - Types of activation functions – Architecture: Feedforward and Feedback – Learning Process: Error Correction Learning –Memory Based Learning – Hebbian Learning – Competitive Learning - Boltzman Learning – Supervised and Unsupervised Learning – Learning Tasks: Pattern Space – Weight Space – Pattern Association – Pattern Recognition – Function Approximation – Control – Filtering - Beamforming – Memory – Adaptation - Statistical Learning Theory – Single Layer Perceptron – Perceptron Learning Algorithm – Perceptron Convergence Theorem – Least Mean Square Learning Algorithm – Multilayer Perceptron – Back Propagation Algorithm – XOR problem – Limitations of Back Propagation Algorithm.

UNIT II RADIAL-BASIS FUNCTION NETWORKS AND SUPPORT VECTOR MACHINES RADIAL BASIS FUNCTION NETWORKS: 9

Cover's Theorem on the Separability of Patterns - Exact Interpolator – Regularization Theory – Generalized Radial Basis Function Networks - Learning in Radial Basis Function Networks - Applications: XOR Problem – Image Classification. Support Vector Machines: Optimal Hyperplane for Linearly Separable Patterns and Nonseparable Patterns – Support Vector Machine for Pattern Recognition – XOR Problem - $\in$-insensitive Loss Function – Support Vector Machines for Nonlinear Regression

UNIT III COMMITTEE MACHINES: 9

Ensemble Averaging - Boosting – Associative Gaussian Mixture Model – Hierarchical Mixture of Experts Model(HME) – Model Selection using a Standard Decision Tree – A Priori and Postpriori Probabilities – Maximum Likelihood Estimation – Learning Strategies for the HME Model - EM Algorithm – Applications of EM Algorithm to HME Model

NEURODYNAMICS SYSTEMS:

Dynamical Systems – Attractors and Stability – Non-linear Dynamical Systems-Lyapunov Stability – Neurodynamical Systems – The Cohen-Grossberg Theorem.

UNIT IV ATTRACTOR NEURAL NETWORKS: 9

Associative Learning – Attractor Neural Network Associative Memory – Linear Associative Memory – Hopfield Network – Content Addressable Memory – Strange Attractors and Chaos - Error Performance of Hopfield Networks - Applications of Hopfield Networks – Simulated Annealing – Boltzmann Machine – Bidirectional Associative Memory – BAM Stability Analysis – Error Correction in BAMs - Memory Annihilation of Structured Maps in BAMS – Continuous BAMs – Adaptive BAMs – Applications

ADAPTIVE RESONANCE THEORY:

Noise-Saturation Dilemma - Solving Noise-Saturation Dilemma – Recurrent On-center – Off-surround Networks – Building Blocks of Adaptive Resonance – Substrate of Resonance Structural Details of Resonance Model – Adaptive Resonance Theory – Applications

UNIT V SELF ORGANISING MAPS: 9

Self-organizing Map – Maximal Eigenvector Filtering – Sanger's Rule – Generalized Learning Law – Competitive Learning - Vector Quantization – Mexican Hat Networks - Self-organizing Feature Maps – Applications

PULSED NEURON MODELS:

Spiking Neuron Model – Integrate-and-Fire Neurons – Conductance Based Models – Computing with Spiking Neurons.

TOTAL: 45 PERIODS

REFERENCES:

1. Satish Kumar, "Neural Networks: A Classroom Approach", Tata McGraw-Hill Publishing Company Limited, New Delhi, 2004.
2. Simon Haykin, "Neural Networks: A Comprehensive Foundation", 2ed., Addison Wesley Longman (Singapore) Private Limited, Delhi, 2001.
3. Martin T.Hagan, Howard B. Demuth, and Mark Beale, "Neural Network Design", Thomson Learning, New Delhi, 2003.
4. James A. Freeman and David M. Skapura, "Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Education (Singapore) Private Limited, Delhi, 2003.

AP9253 ROBOTICS L T P C
3 0 0 3

UNIT I INTRODUCTION TO ROBOTICS 9

Motion - Potential Function, Road maps, Cell decomposition and Sensor and sensor planning. Kinematics. Forward and Inverse Kinematics - Transformation matrix and DH transformation. Inverse Kinematics - Geometric methods and Algebraic methods. Non-Holonomic constraints.

UNIT II COMPUTER VISION 9

Projection - Optics, Projection on the Image Plane and Radiometry. Image Processing - Connectivity, Images-Gray Scale and Binary Images, Blob Filling, Thresholding, Histogram. Convolution - Digital Convolution and Filtering and Masking Techniques. Edge Detection - Mono and Stereo Vision.

UNIT III SENSORS AND SENSING DEVICES 9

Introduction to various types of sensor. Resistive sensors. Range sensors - Ladar (laser distance and ranging), Sonar, Radar and Infra-red. Introduction to sensing - Light sensing, Heat sensing, Touch sensing and Position sensing.

UNIT IV ARTIFICIAL INTELLIGENCE 9

Uniform Search strategies - Breadth first, Depth first, Depth limited, Iterative and deepening depth first search and Bidirectional search. The A* algorithm . Planning - State-Space Planning , Plan-Space Planning, Graphplan/SatPlan and their Comparison, Multi-agent planning 1, and Multi-agent planning 2, Probabilistic Reasoning - Bayesian Networks, Decision Trees and Bayes net inference

UNIT V INTEGRATION TO ROBOT 9

Building of 4 axis or 6 axis robot - Vision System for pattern detection - Sensors for obstacle detection - AI algorithms for path finding and decision making

TOTAL: 45 PERIODS

REFERENCES:

1. Duda, Hart and Stork, Pattern Recognition. Wiley-Interscience, 2000.
2. Mallot, Computational Vision: Information Processing in Perception and Visual Behavior. Cambridge, MA: MIT Press, 2000.
3. Artificial Intelligence-A Modern Approach By Stuart Russell and Peter Norvig, Pearson Education Series in Artificial Intelligence, 2004
4. Fundamentals of Robotics, Analysis and control By Robert Schilling and Craig, Hall of India Private Limied, New Delhi, 2003.
5. Computer Vision, A modern Approach By Forsyth and Ponce, Person Education, 2003.

VL9211 DSP INTEGRATED CIRCUITS L T P C
3 0 0 3

UNIT I DSP INTEGARTED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES 9

Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

UNIT II DIGITAL SIGNAL PROCESSING 9

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

UNIT III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT IV DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES 9

DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs**.**

UNIT V ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN 9

Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies. Cordic algorithm.

TOTAL: 45 PERIODS

REFERENCES:

1. Lars Wanhammer, “DSP Integrated Circuits”, 1999 Academic press, New York
2. A.V.Oppenheim et.al, “Discrete-time Signal Processing”, Pearson Education, 2000.
3. Emmanuel C. Ifeachor, Barrie W. Jervis, “ Digital signal processing – A practical approach”, Second Edition, Pearson Education, Asia.
4. Keshab K.Parhi, “VLSI Digital Signal Processing Systems design and Implementation”, John Wiley & Sons, 1999.

VL9261 ASIC DESIGN L T P C
3 0 0 3

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture .

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 9

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL: 45 PERIODS

REFERENCES:

1. M.J.S .Smith, "Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997.
2. Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.
3. Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.
4. R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House Publishers, 2000.
5. F. Nekoogar. Timing Verification of Application-Specific Integrated Circuits (ASICs). Prentice Hall PTR, 1999.

AP9260 DESIGN AND ANALYSIS OF ALGORITHMS L T P C

3 0 0 3

UNIT I INTRODUCTION 9

Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

UNIT II DESIGN TECHNIQUES 9

Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

UNIT III SEARCHING AND SORTING 9

Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior

UNIT IV GRAPH ALGORITHMS 9

Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms, max-flow min cut theorem, Steiglitz's link deficit algorithm.

UNIT V SELECTED TOPICS 9

NP Completeness Approximation Algorithms, NP Hard Problems, Strasseu's Matrix Multiplication Algorithms, Magic Squares, Introduction To Parallel Algorithms and Genetic Algorithms, Monte-Carlo Methods, Amortised Analysis.

TOTAL: 45PERIODS

REFERENCES:

1. Sara Baase, "Computer Algorithms : Introduction to Design and Analysis", Addison Wesley, 1988.
2. T.H.Cormen, C.E.Leiserson and R.L.Rivest, "Introduction to Algorithms", Mc Graw Hill, 1994.
3. E.Horowitz and S.Sahni, "Fundamentals of Computer Algorithms", Galgotia Publications, 1988.
4. D.E.Goldberg, "Genetic Algorithms : Search Optimization and Machine Learning", Addison Wesley, 1989.

NE9251 RELIABILITY ENGINEERING L T P C
3 0 0 3

UNIT I PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE 9

Statistical distribution , statistical confidence and hypothesis testing ,probability plotting techniques – Weibull, extreme value ,hazard, binomial data; Analysis of load – strength interference , Safety margin and loading roughness on reliability.

UNIT II RELIABILITY PREDICTION, MODELLING AND DESIGN 9

Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis ,petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY 9

Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV RELIABILITY TESTING AND ANALYSIS 9

Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V MANUFACTURE AND RELIABILITY MAQNAGEMENT 9

Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes , reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

TOTAL: 45 PERIODS

REFERENCES:

1. Patrick D.T. O'Connor, David Newton and Richard Bromley, Practical Reliability Engineering, Fourth edition, John Wiley & Sons, 2002
2. David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, New York, "AT & T Reliability Manual", 5th Edition, 1998.
3. Gregg K. Hobbs, "Accelerated Reliability Engineering - HALT and HASS", John Wiley & Sons, New York, 2000.
4. Lewis, "Introduction to Reliability Engineering", 2nd Edition, Wiley International, 1996.

AP9256	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN	L T P C 3 0 0 3

UNIT I EMI/EMC CONCEPTS 9

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES 9

Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES 9

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV EMC DESIGN OF PCBS 9

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V EMI MEASUREMENTS AND STANDARDS 9

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

TOTAL: 45 PERIODS

REFERENCES:

1. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, Newyork, 1996.
2. Henry W.Ott.,"Noise Reduction Techniques in Electronic Systems", A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
3. Bemhard Keiser, "Principles of Electromagnetic Compatibility", 3rd Ed, Artech house, Norwood, 1986.
4. C.R.Paul,"Introduction to Electromagnetic Compatibility" , John Wiley and Sons, Inc, 1992.
5. Don R.J.White Consultant Incorporate, "Handbook of EMI/EMC" , Vol I-V, 1988.

CP9212 HIGH PERFORMANCE COMPUTER NETWORKS L T P C
3 0 0 3

UNIT I INTRODUCTION 9

Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing. SONET – DWDM – DSL – ISDN – BISDN,ATM.

UNIT II MULTIMEDIA NETWORKING APPLICATIONS 9

Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services – RSVP- differentiated services.

UNIT III ADVANCED NETWORKS CONCEPTS 9

VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN.MPLS-operation, Routing, Tunneling and use of FEC, Traffic Engineering, MPLS based VPN, overlay networks-P2P connections.

UNIT IV TRAFFIC MODELLING 8

Little's theorem, Need for modeling , Poisson modeling and its failure, Non- poisson models, Network performance evaluation.

UNIT V NETWORK SECURITY AND MANAGEMENT 10

Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and: fire walls – attacks and counter measures – security in many layers. Infrastructure for network management – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1

TOTAL:45 PERIODS

REFERENCES:

1. J.F. Kurose & K.W. Ross,"Computer Networking- A top down approach featuring the internet", Pearson, 2nd edition, 2003.
2. Walrand .J. Varatya, High performance communication network, Morgan Kauffman – Harcourt Asia Pvt. Ltd. 2nd Edition, 2000.
3. LEOM-GarCIA, WIDJAJA, "Communication networks", TMH seventh reprint 2002.
4. Aunurag kumar, D. MAnjunath, Joy kuri, "Communication Networking", Morgan Kaufmann Publishers, 1ed 2004.
5. Hersent Gurle & petit, "IP Telephony, packet Pored Multimedia communication Systems", Pearson education 2003.
6. Fred Halsall and Lingana Gouda Kulkarni,"Computer Networking and the Internet" fifth edition, Pearson education
7 Nader F.Mir ,Computer and Communication Networks, first edition.
8. Larry l.Peterson & Bruce S.David, "Computer Networks: A System Approach"-1996

AP9258 **RF SYSTEM DESIGN** **L T P C**
3 0 0 3

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES 9

CMOS: Introduction to MOSFET Physics – Noise: Thermal, shot, flicker, popcorn noise
Transceiver Specifications: Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link
Transceiver Architectures: Receiver: Homodyne, Heterodyne, Image reject, Low IF Architectures – Transmitter: Direct upconversion, Two step upconversion

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS 9

S-parameters with Smith chart – Passive IC components - Impedance matching networks Amplifiers: Common Gate, Common Source Amplifiers – OC Time constants in bandwidth estimation and enhancement – High frequency amplifier design
Low Noise Amplifiers: Power match and Noise match – Single ended and Differential LNAs – Terminated with Resistors and Source Degeneration LNAs.

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS 9

Feedback Systems: Stability of feedback systems: Gain and phase margin, Root-locus techniques – Time and Frequency domain considerations – Compensation
Power Amplifiers: General model – Class A, AB, B, C, D, E and F amplifiers – Linearisation Techniques – Efficiency boosting techniques – ACPR metric – Design considerations

UNIT IV PLL AND FREQUENCY SYNTHESIZERS 9

PLL: Linearised Model – Noise properties – Phase detectors – Loop filters and Charge pumps Frequency Synthesizers: Integer-N frequency synthesizers – Direct Digital Frequency synthesizers

UNIT V MIXERS AND OSCILLATORS 9

Mixer: characteristics – Non-linear based mixers: Quadratic mixers – Multiplier based mixers: Single balanced and double balanced mixers – subsampling mixers
Oscillators: Describing Functions, Colpitts oscillators – Resonators – Tuned Oscillators – Negative resistance oscillators – Phase noise

TOTAL: 45 PERIODS

TEXT BOOKS:

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004
2. B.Razavi, “RF Microelectronics”, Pearson Education, 1997
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997
4. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001.

VL9252 **LOW POWER VLSI DESIGN** **L T P C**
3 0 0 3

UNIT I POWER DISSIPATION IN CMOS 9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design.

UNIT II POWER OPTIMIZATION 9

Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques

UNIT IV POWER ESTIMATION 9

Power estimation techniques – Logic level power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9

Synthesis for low power –Behavioral level transforms- Software design for low power -

TOTAL : 45 PERIODS

REFERENCES:

1. K.Roy and S.C. Prasad , LOW POWER CMOS VLSI circuit design, Wiley,2000
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, DESIGNING CMOS CIRCUITS FOR LOW POWER, Kluwer,2002
3. J.B. Kuo and J.H Lou, Low voltage CMOS VLSI Circuits, Wiley 1999.
4. A.P.Chandrakasan and R.W. Broadersen, Low power digital CMOS design, Kluwer,1995.
5. Gary Yeap, Practical low power digital VLSI design, Kluwer,1998.
6. Abdellatif Bellaouar,Mohamed.I. Elmasry, Low power digital VLSI design,s Kluwer, 1995.
7. James B. Kuo, Shin – chia Lin, Low voltage SOI CMOS VLSI Devices and Circuits. John Wiley and sons, inc 2001

VL9253 VLSI SIGNAL PROCESSING L T P C
3 0 0 3

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL : 45 PERIODS

REFERENCES:

1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004

VL9254 ANALOG VLSI DESIGN L T P C
3 0 0 3

UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGESIGNAL PROCESSING 9

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOSTransistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING 9

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS 9

First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma-Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filters-mechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS 9

Fault modelling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses-Design for Electron -Beam Testablity-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT 9

Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

TOTAL : 45 PERIODS

REFERENCES:

1. Mohammed Ismail, Terri Fiez, “Analog VLSI signal and Information Processing ", McGraw-Hill International Editons, 1994.
2. Malcom R.Haskard, Lan C.May, “Analog VLSI Design - NMOS and CMOS ", Prentice Hall, 1998.
3. Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990.
4. Jose E.France, Yannis Tsividis, “Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994

VL9221 CAD FOR VLSI CIRCUITS L T P C
3 0 0 3

UNIT I VLSI DESIGN METHODOLOGIES 9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II DESIGN RULES 9

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

UNIT III FLOOR PLANNING 9

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION 9

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V MODELLING AND SYNTHESIS 9

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

TOTAL: 45 PERIODS

REFERENCES :

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

AP9259 HARDWARE SOFTWARE CO-DESIGN L T P C
3 0 0 3

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems , Hardware/Software Co-Design , Co-Design for System Specification and Modelling , Co-Design for Heterogeneous Implementation - Processor Synthesis , Single-Processor Architectures with one ASIC , Single-Processor Architectures with many ASICs, Multi-Processor Architectures , Comparison of Co-Design Approaches , Models of Computation ,Requirements for Embedded System Specification .

UNIT II HARDWARE/SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph , Formulation of the HW/SW Partitioning Problem , Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms .

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments ,Future Developments in Emulation and Prototyping ,Target Architecture-Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification , Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation

TOTAL: 45 PERIODS

REFERENCES:

1. Ralf Niemann , “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup , Wayne Wolf ,”Hardware/Software Co-Design: Principles and Practice” , Kluwer Academic Pub,1997.
3. Giovanni De Micheli , Rolf Ernst Morgon,” Reading in Hardware/Software Co-Design “ Kaufmann Publishers,2001.